B44AS8G53222B-SE51
DDR4 SO-DIMM 8GB 1Rx8

General Description

This document describes Biwin's B44AS8G53222B-SE51 1Gig x 64 1Rank 8GB DDR4-3200 CL22 1.2V SDRAM Unbuffered SODIMM (Small Outline Dual In-Line Memory Module) product.

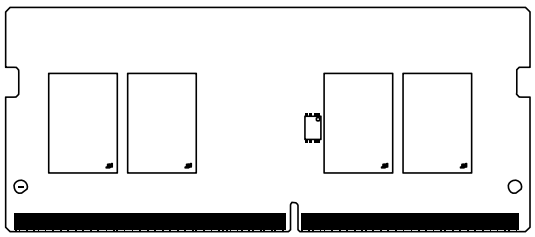
This product design specification reference JEDEC standard (No. 21C DDR4 SDRAM DIMM Design Specification) raw-card A2.

This product's outline reference JEDEC design MO310.

Features

- DDR4 functionality and operations supported as defined in the component data sheet
- 260-pin, small-outline dual in-line memory module (SO-DIMM)
- Fast data transfer rates: PC4-3200
- 8GB (1 Gig x 64)
- V_{DD} = 1.20V (NOM)
- V_{PP} = 2.5V (NOM)
- V_{DD} SPD = 2.5V (NOM)
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Low-power auto self refresh (LPASR)
- Data bus inversion (DBI) for data bus
- On-die V_{REFDQ} generation and calibration
- Single-rank
- On-board I²C serial presence-detect (SPD) EEPROM
- 16 internal banks; 4 groups of 4 banks each
- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the mode register set (MRS)
- Selectable BC4 or BL8 on-the-fly (OTF)
- Gold edge contacts (30μ")
- Halogen-free
- Fly-by topology
- Terminated control command and address bus

Options



- Operating temperature
  – Commercial (0°C ≤ T_{OPER} ≤ +85°C)
- Storage temperature
  – - 55°C ≤ T_{STG} ≤ +100°C
- Package: 260-pin DIMM (halogen-free)
- Frequency/CAS latency
  – 0.625ns @ CL = 22 (DDR4-3200)

Contents

1. Ordering Information and Key Features

1）Ordering Information

Part Number	Capacity	Organization	Component Composition	Number of Rank	Height
B44AS8G53222B-SE51	8GB	1Gig x 64	1Gigx8*8	1	30.00mm

DRAM：K4A8G085WE-BCWE

2）Key Features

Speed	DDR4-3200AA	Unit
	22-22-22	
tCK (min)	0.625	ns
CAS Latency	22	nCK
tAA（min）	13.75	ns
tRCD (min)	13.75	ns
tRP (min)	13.75	ns
tRAS （min）	32	ns
tRC （min）	45.75	ns

Note :

1. Before purchase and assembly your computer, please consult motherboard and CPU manufacture, review the motherboard and CPU manufacture website, check the hardware Spec, make sure the hardware support the memory module rated speed and latency.
2. Average Refresh Period 7.8us at lower then T_{CASE} 85℃, 3.9us at 85℃< T_{CASE} < 95℃.

2. Addressing

Parameter	8GB
Row address	64K A[15:0]
Column address	1K A[9:0]
Device bank group address	4 BG[1:0]
Device bank address per group	4 BA[1:0]
Device configuration	8Gb (1 Gig x 8), 16 banks
Module rank address	CS0_n

3. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Notes
V_{DD}	V_{DD} supply voltage relative to V_{SS}	- 0.3	1.5	V	1
V_{DDQ}	V_{DDQ} supply voltage relative to V_{SS}	- 0.3	1.5	V	1
V_{PP}	Voltage on V_{PP} pin relative to V_{SS}	- 0.3	3	V	2
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	- 0.3	1.5	V	

4.Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units	Notes
V_{DD}	V_{DD} supply voltage	1.14	1.2	1.26	V	1
V_{PP}	DRAM activating power supply	2.375	2.5	2.75	V	2
V_{REFCA}(DC)	Input reference voltage command/ address bus	0.49 × V_{DD}	0.5 × V_{DD}	0.51 × V_{DD}	V	3
I_{VTT}	Termination reference current from V_{TT}	- 500	–	500	mA	
V_{TT}	Termination reference voltage (DC) – command/address bus	0.49 × V_{DD} - 20mV	0.5 × V_{DD}	0.51 × V_{DD} + 20mV	V	4
I_{IN}	Input leakage current; any input excluding ZQ; 0V < V_{IN} < 1.1V	- 2.0	–	2	µA	5
I_{ZQ}	Input leakage current; ZQ	- 50.0	–	10	µA	5,6
I_{OZpd}	Output leakage current; V_{OUT} = V_{DD}; DQ is High-Z	–	–	10	µA	
I_{OZpu}	Output leakage current; V_{OUT} = V_{SS}; DQ is High-Z; ODT is disabled with ODT input HIGH	- 50.0	–	–	µA	
I_{VREFCA}	V_{REFCA} leakage; V_{REFCA} = V_{DD}/2 (after DRAM is initialized)	- 2.0	–	2	µA	5

Notes:

1. V_{DDQ} tracks with V_{DD}; V_{DDQ} and V_{DD} are tied together.
2. V_{PP} must be greater than or equal to V_{DD} at all times.
3. V_{REFCA} must not be greater than 0.6 x V_{DD}. When V_{DD} is less than 500mV, V_{REF} may be less than or equal to 300mV.
4. V_{TT} termination voltages in excess of the specification limit adversely affect the voltage margins of command and address signals and reduce timing margins.
5. Multiply by the number of DRAM die on the module.
6. Tied to ground. Not connected to edge connector.

5. Architecture

x8 Package Ball out (Top view) : 78ball FBGA Package

	1	2	3	4	5	6	7	8	9	
A	VDD	VSSQ	TDQS_c				DM_n/DBI_n TDQS_t	VSSQ	VSS	A
B	VPP	VDDQ	DQS_c				DQ1	VDDQ	ZQ	B
C	VDDQ	DQ0	DQS_t				VDD	VSS	VDDQ	C
D	VSSQ	DQ4	DQ2				DQ3	DQ5	VSSQ	D
E	VSS	VDDQ	DQ6				DQ7	VDDQ	VSS	E
F	VDD	ODT1	ODT				CK_t	CK_c	VDD	F
G	VSS	CKE1	CKE				CS_n	CS1_n	TEN	G
H	VDD	WE_n A14	ACT_n				CAS_n A15	RAS_n A16	VSS	H
J	VREFCA	BG0	A10 AP				A12 BC_n	BG1	VDD	J
K	VSS	BA0	A4				A3	BA1	VSS	K
L	RESET_n	A6	A0				A1	A5	ALERT_n	L
M	VDD	A8	A2				A9	A7	VPP	M
N	VSS	A11	PAR				A17	A13	VDD	N
	1	2	3	4	5	6	7	8	9	

6. Pin Assignments

260-Pin DDR4 SODIMM Front								260-Pin DDR4 SODIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VSS	67	DQ29	133	A1	199	DM5_n/ DBI5_n	2	VSS	68	VSS	134	EVENT_n, NF	200	DQS5_t
3	DQ5	69	VSS	135	VDD	201	VSS	4	DQ4	70	DQ24	136	VDD	202	VSS
5	VSS	71	DQ25	137	CK0_t	203	DQ46	6	VSS	72	VSS	138	CK1_t/NF	204	DQ47
7	DQ1	73	VSS	139	CK0_c	205	VSS	8	DQ0	74	DQS3_c	140	CK1_c/NF	206	VSS
9	VSS	75	DM3_n/ DBI3_n	141	VDD	207	DQ42	10	VSS	76	DQS3_t	142	VDD	208	DQ43
11	DQS0_c	77	VSS	143	PARITY	209	VSS	12	DM0_n/ DBI0_n	78	VSS	144	A0	210	VSS
13	DQS0_t	79	DQ30	145	BA1	211	DQ52	14	VSS	80	DQ31	146	A10/AP	212	DQ53
15	VSS	81	VSS	147	VDD	213	VSS	16	DQ6	82	VSS	148	VDD	214	VSS
17	DQ7	83	DQ26	149	CS0_n	215	DQ49	18	VSS	84	DQ27	150	BA0	216	DQ48
19	VSS	85	VSS	151	WE_n/ A14	217	VSS	20	DQ2	86	VSS	152	RAS_n/ A16	218	VSS
21	DQ3	87	CB5/NC	153	VDD	219	DQS6_c	22	VSS	88	CB4/NC	154	VDD	220	DM6_n/ DBI6_n
23	VSS	89	VSS	155	ODT0	221	DQS6_t	24	DQ12	90	VSS	156	CAS_n/ A15	222	VSS
25	DQ13	91	CB1/NC	157	CS1_n/ NC	223	VSS	26	VSS	92	CB0/NC	158	A13	224	DQ54
27	VSS	93	VSS	159	VDD	225	DQ55	28	DQ8	94	VSS	160	VDD	226	VSS
29	DQ9	95	DQS8_c/ NC	161	ODT1/ NC	227	VSS	30	VSS	96	DM8_n/ DBI_n/NC	162	C0/ CS2_n/N C	228	DQ50
31	VSS	97	DQS8_t/ NC	163	VDD	229	DQ51	32	DQS1_c	98	VSS	164	VREFCA	230	VSS
33	DM1_n/ DBI_n	99	VSS	165	C1, CS3_n, NC	231	VSS	34	DQS1_t	100	CB6/NC	166	SA2	232	DQ60
35	VSS	101	CB2/NC	167	VSS	233	DQ61	36	VSS	102	VSS	168	VSS	234	VSS
37	DQ15	103	VSS	169	DQ37	235	VSS	38	DQ14	104	CB7/NC	170	DQ36	236	DQ57
39	VSS	105	CB3/NC	171	VSS	237	DQ56	40	VSS	106	VSS	172	VSS	238	VSS
41	DQ10	107	VSS	173	DQ33	239	VSS	42	DQ11	108	RESET_n	174	DQ32	240	DQS7_c
43	VSS	109	CKE0	175	VSS	241	DM7_n/ DBI7_n	44	VSS	110	CKE1/ NC	176	VSS	242	DQS7_t
45	DQ21	111	VDD	177	DQS4_c	243	VSS	46	DQ20	112	VDD	178	DM4_n/ DBI4_n	244	VSS

6. Pin Assignments

260-Pin DDR4 SODIMM Front								260-Pin DDR4 SODIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
47	VSS	113	BG1	179	DQS4_t	245	DQ62	48	VSS	114	ACT_n	180	VSS	246	DQ63
49	DQ17	115	BG0	181	VSS	247	VSS	50	DQ16	116	ALERT_n	182	DQ39	248	VSS
51	VSS	117	VDD	183	DQ38	249	DQ58	52	VSS	118	VDD	184	VSS	250	DQ59
53	DQS2_c	119	A12	185	VSS	251	VSS	54	DM2_n/ DBI2_n	120	A11	186	DQ35	252	VSS
55	DQS2_t	121	A9	187	DQ34	253	SCL	56	VSS	122	A7	188	VSS	254	SDA
57	VSS	123	VDD	189	VSS	255	VDDSPD	58	DQ22	124	VDD	190	DQ45	256	SA0
59	DQ23	125	A8	191	DQ44	257	VPP	60	VSS	126	A5	192	VSS	258	VTT
61	VSS	127	A6	193	VSS	259	VPP	62	DQ18	128	A4	194	DQ41	260	SA1
63	DQ19	129	VDD	195	DQ40	–	–	64	VSS	130	VDD	196	VSS	–	–
65	VSS	131	A3	197	VSS	–	–	66	DQ28	132	A2	198	DQS5_c	–	–

7. Pin Description

The pin description table below is a comprehensive list of all possible pins for DDR4 modules. All pins listed may not be supported on this module. Seeing the Functional Block Diagram for pins specific to this module.

Symbol	Type	Description
Ax	Input	**Address inputs:** Provide the row address for ACTIVATE commands and the column address for READ/WRITE commands in order to select one location out of the memory array in the respec- tive bank (A10/AP, A12/BC_n, WE_n/A14, CAS_n/A15, and RAS_n/A16 have additional functions; see individual entries in this table). The address inputs also provide the op-code during the MODE REGISTER SET command. A17 is only defined for x4 SDRAM.
A10/AP	Input	**Auto pre-charge:** A10 is sampled during READ and WRITE commands to determine whether an auto pre-charge should be performed on the accessed bank after a READ or WRITE operation (HIGH = auto pre-charge; LOW = no auto pre-charge). A10 is sampled during a PRECHARGE command to determine whether the pre-charge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be pre-charged, the bank is selected by the bank group and bank addresses.
A12/BC_n	Input	**Burst chop:** A12/BC_n is sampled during READ and WRITE commands to determine if burst chop (on-the-fly) will be performed (HIGH = no burst chop; LOW = burst chopped). See Command Truth Table in the DDR4 component data sheet.
ACT_n	Input	**Command input:** ACT_n defines the ACTIVATE command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15, and WE_n/A14 are considered as row address A16, A15, and A14. See Command Truth Table.
BAx	Input	**Bank address inputs:** Define the bank (with a bank group) to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. Also determine which mode register is to be accessed during a MODE REGISTER SET command.
BGx	Input	**Bank group address inputs:** Define the bank group to which a REFRESH, ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. Also determine which mode register is to be accessed during a MODE REGISTER SET command. BG[1:0] are used in the x4 and x8 configurations. x16-based SDRAM only has BG0.
C0, C1, C2 (RDIMM/LRDIMM only)	Input	**Chip ID:** These inputs are used only when devices are stacked; that is, 2H, 4H, and 8H stacks for x4 and x8 configurations using through-silicon vias (TSVs). These pins are not used in the x16 configuration. Some DDR4 modules support a traditional DDP package, which uses CS1_n, CKE1, and ODT1 to control the second die. All other stack configurations, such as a 4H or 8H, are assumed to be single-load (master/slave) type configurations where C0, C1, and C2 are used as chip ID selects in conjunction with a single CS_n, CKE, and ODT. Chip ID is considered part of the command code.
CKx_t CKx_c	Input	**Clock:** Differential clock inputs. All address, command, and control input signals are sampled on the crossing of the positive edge of CK_t and the negative edge of CK_c.

7. Pin Description

Symbol	Type	Description
CKEx	Input	**Clock enable:** CKE HIGH activates and CKE LOW deactivates the internal clock signals, device input buffers, and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), or active power-down (row active in any bank). CKE is asynchronous for self refresh exit. After VREFCA has become stable during the power-on and initialization sequence, it must be maintained during all operations (including SELF REFRESH). CKE must be maintained HIGH throughout read and write accesses. Input buffers (excluding CK_t, CK_c, ODT, RESET_n and CKE) are disabled during power-down. Input buffers (excluding CKE and RESET_n) are disabled during self refresh.
CSx_n	Input	**Chip select:** All commands are masked when CS_n is registered HIGH. CS_n provides external rank selection on systems with multiple ranks. CS_n is considered part of the command code (CS2_n and CS3_n are not used on UDIMMs).
ODTx	Input	**On-die termination:** ODT (registered HIGH) enables termination resistance internal to the DDR4 SDRAM. When enabled, ODT (RTT) is applied only to each DQ, DQS_t, DQS_c, DM_n/ DBI_n/TDQS_t, and TDQS_c signal for x4 and x8 configurations (when the TDQS function is ena- bled via the mode register). For the x16 configuration, RTT is applied to each DQ, DQSU_t, DQSU_c, DQSL_t, DQSL_c, UDM_n, and LDM_n signal. The ODT pin will be ignored if the mode registers are programmed to disable RTT.
PARITY	Input	**Parity for command and address:** This function can be enabled or disabled via the mode register. When enabled in MR5, the DRAM calculates parity with ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, BG[1:0], BA[1:0], A[16:0]. Input parity should be maintained at the rising edge of the clock and at the same time as command and address with CS_n LOW.
RAS_n/A16 CAS_n/A15 WE_n/A14	Input	**Command inputs:** RAS_n/A16, CAS_n/A15, and WE_n/A14 (along with CS_n) define the command and/or address being entered and have multiple functions. For example, for activation with ACT_n LOW, these are addresses like A16, A15, and A14, but for a non-activation command with ACT_n HIGH, these are command pins for READ, WRITE, and other commands de- fined in Command Truth Table.
RESET_n	CMOS Input	**Active LOW asynchronous reset:** Reset is active when RESET_n is LOW and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation.
SAx	Input	**Serial address inputs:** Used to configure the temperature sensor/SPD EEPROM address range on the I^2C bus.
SCL	Input	**Serial clock for temperature sensor/SPD EEPROM:** Used to synchronize communication to and from the temperature sensor/SPD EEPROM on the I^2C bus.
DQx, CBx	I/O	**Data input/output and check bit input/output:** Bidirectional data bus. DQ represents DQ[3:0], DQ[7:0], and DQ[15:0] for the x4, x8, and x16 configurations, respectively. If cyclic re dundancy checksum (CRC) is enabled via the mode register, the CRC code is added at the end of the data burst. Any one or all of DQ0, DQ1, DQ2, or DQ3 may be used for monitoring of inter- nal VREF level during test via mode register setting MR[4] A[4 = HIGH; training times change when enabled.
DM_n/DBI_n/ TDQS_t (DMU_n, DBIU_n), (DML_n/ DBIl_n)	I/O	**Input data mask and data bus inversion:** DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a write access. DM_n is sampled on both edges of DQS. DM is multiplexed with the DBI function by the mode register A10, A11, and A12 settings in MR5. For a x8 device, the function of DM or TDQS is enabled by the mode register A11 setting in MR1. DBI_n is an input/output identifying whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/ output after inversion inside the DDR4 device and not inverted if DBI_n is HIGH. TDQS is only supported in x8 SDRAM configurations (TDQS is not valid for UDIMMs).

7. Pin Description

Symbol	Type	Description
SDA	I/O	**Serial Data:** Bidirectional signal used to transfer data in or out of the EEPROM or EEPROM/TS combo device.
DQS_t DQS_c DQSU_t DQSU_c DQSL_t DQSL_c	I/O	**Data strobe:** Output with read data, input with write data. Edge-aligned with read data, centered-aligned with write data. For x16 configurations, DQSL corresponds to the data on DQ[7:0], and DQSU corresponds to the data on DQ[15:8]. For the x4 and x8 configurations, DQS corresponds to the data on DQ[3:0] and DQ[7:0], respectively. DDR4 SDRAM supports a differential data strobe only and does not support a single-ended data strobe.
ALERT_n	Output	**Alert output:** Possesses functions such as CRC error flag and command and address parity error flag as output signal. If a CRC error occurs, ALERT_n goes LOW for the period time interval and returns HIGH. If an error occurs during a command address parity check, ALERT_n goes LOW un- til the on-going DRAM internal recovery transaction is complete. During connectivity test mode, this pin functions as an input. Use of this signal is system-dependent. If not connected as signal, ALERT_n pin must be connected to VDD on DIMMs.
EVENT_n	Output	**Temperature event:** The EVENT_n pin is asserted by the temperature sensor when critical tem- perature thresholds have been exceeded. This pin has no function (NF) on modules without temperature sensors.
TDQS_t TDQS_c (x8 DRAM-based RDIMM only)	Output	**Termination data strobe:** When enabled via the mode register, the DRAM device enables the same RTT termination resistance on TDQS_t and TDQS_c that is applied to DQS_t and DQS_c. When the TDQS function is disabled via the mode register, the DM/TDQS_t pin provides the data mask (DM) function, and the TDQS_c pin is not used. The TDQS function must be disabled in the mode register for both the x4 and x16 configurations. The DM function is supported only in x8 and x16 configurations. DM DBI, and TDQS are a shared pin and are enabled/disabled by mode register settings. For more information about TDQS, see the DDR4 DRAM component data sheet (TDQS_t and TDQS_c are not valid for UDIMMs).
V_{DD}	Supply	**Module power supply:** 1.2V (TYP).
V_{PP}	Supply	**DRAM activating power supply:** 2.5V – 0.125V / + 0.250V.
V_{REFCA}	Supply	Reference voltage for control, command, and address pins.
V_{SS}	Supply	Ground.
V_{TT}	Supply	Power supply for termination of address, command, and control $V_{DD}/2$.
V_{DD}SPD	Supply	Power supply used to power the I^2C bus for SPD.
RFU	–	Reserved for future use.
NC	–	**No connect:** No internal electrical connection is present.
NF	–	**No function:** May have internal connection present, but has no function.

8. Input / Output Functional Description

Item	Symbol	Type	Function
1	CK0_t, CK0_c CK1_t, CK1_c	Input	**Clock:** CK_t and CK_ care differential clock inputs. crossing of the positive edge of CK_t and negative edge of CK_c.
2	CKE0, CKE1	Input	**Clock Enable:** CKE HIGH activates and CKE LOW deactivates internal clock signals and device input buffers and output drivers. Taking CKE LOW provides Pre-charge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t,CK_c, ODT and CKE, are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
3	CS0_n, CS1_n, CS2_n, CS3_n,	Input	**Chip Select:** All commands are masked when CS_n is r selection on systems with multiple Ranks. CS_n is considered part of the command code. egistered HIGH. CS_n provides for external Rank
4	C0, C1	Input	**Chip ID:** Chip ID is only used for 3DS for 2 and 4 high stack via TSV to select each slice of stacked component. Chip ID is considered part of the command code.
5	ODT0, ODT1	Input	**On Die Termination:** ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c and DM_n/DBI_n/, signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
6	ACT_n	Input	**Activation Command Input:** ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/A14 will be considered as Row Address A16, A15, and A14
7	RAS_n/A16. CAS_n/A15. WE_n/A14.	Input	**Command Inputs:** RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, these are Addresses like A16 A15, and A14 but for non-activation command with ACT_n High, these are Command pins for Read, Write, and other command defined in command truth table

8. Input / Output Functional Description

Item	Symbol	Type	Function
8	DM_n/ DBI_n	Input/ Output	**Input Data Mask and Data Bus Inversion:** DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. DM is muxed with DBI function. DBI_n is an input/output identifying whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if DBI_n is HIGH.
9	BG0 - BG1	Input	**Bank Group Inputs:** BG0 - BG1 define which bank group an Active, Read, Write, or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. For x4/x8 based SDRAMs, BG0 and BG1 are valid. For x16 based SDRAM components, only BG0 is valid.
10	BA0 - BA1	Input	**Bank Address Inputs:** BA0 - BA1 define to which bank an Active, Read, Write, or Pre-charge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
11	A0 - A16	Input	**Address Inputs:** Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions. See other rows. The address inputs also provide the op-code during Mode Register Set commands.
12	A10 / AP	Input	**Auto-pre-charge:** A10 is sampled during Read/Write commands to determine whether Auto-pre-charge should be performed to the accessed bank after the Read/Write operation. (HIGH: Auto pre-charge; LOW: no Auto-pre-charge). A10 is sampled during a Pre-charge command to determine whether the Pre-charge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be pre-charged, the bank is selected by bank addresses.
13	A12 / BC_n	Input	**Burst Chop:** A12/BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
14	RESET_n	CMOS Input	**Active Low Asynchronous Reset:** Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation.
15	DQ	Input/ Output	**Data Input/ Output:** Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0-DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific Data Sheets to determine which DQ is used.

8. Input / Output Functional Description

Item	Symbol	Type	Function
16	DQS_t, DQS_c	Input/Output	**Data Strobe:** output with read data, input with write data. Edge-aligned with read data, centered in write
17	PARITY	Input	**Command and Address Parity Input:** DDR4 Supports Even Parity check in DRAMs with MR setting. Once it's enabled via Register in MR5, then SDRAM calculates Parity with ACT_n, RAS_n/A16, CAS_n/A15,WE_n/A14, BG0-BG1, BA0-BA1, A16-A0. Input parity should be maintained at the rising edge of the clock and at the same time with command & address with CS_n LOW
18	ALERT_n	Output	**ALERT:** It has multi functions such as CRC error flag, Command and Address Parity error flag as Output signal. If there is error in CRC, then ALERT_n goes LOW for the period time interval and goes back HIGH.If there is error in Command Address Parity Check, then ALERT_n goes LOW for A relatively long period until on-going DRAM internal recovery transaction is complete. During Connectivity Test mode, this pin functions as an input.Using this signal or not is dependent on the system.
19	SA0-SA1		Device address for the SPD.
20	RFU		Reserved for Future Use. No on-DIMM electrical connection is present.
21	NC		**No Connect:** No on-DIMM electrical connection is present.
22	$V_{DD}1$	Supply	**Power Supply:** 1.2 V +/- 0.06 V
23	V_{SS}	Supply	Ground
24	$V_{TT}2$	Supply	**Power Supply:** 0.6 V
25	V_{PP}	Supply	**DRAM Activating Power Supply:** 2.5 V (2.375 V min, 2.75 V max)
26	V_{REFCA}	Supply	Reference voltage for CA
27	V_{DD}SPD	Supply	Power supply used to power the I^2C bus on the SPD.

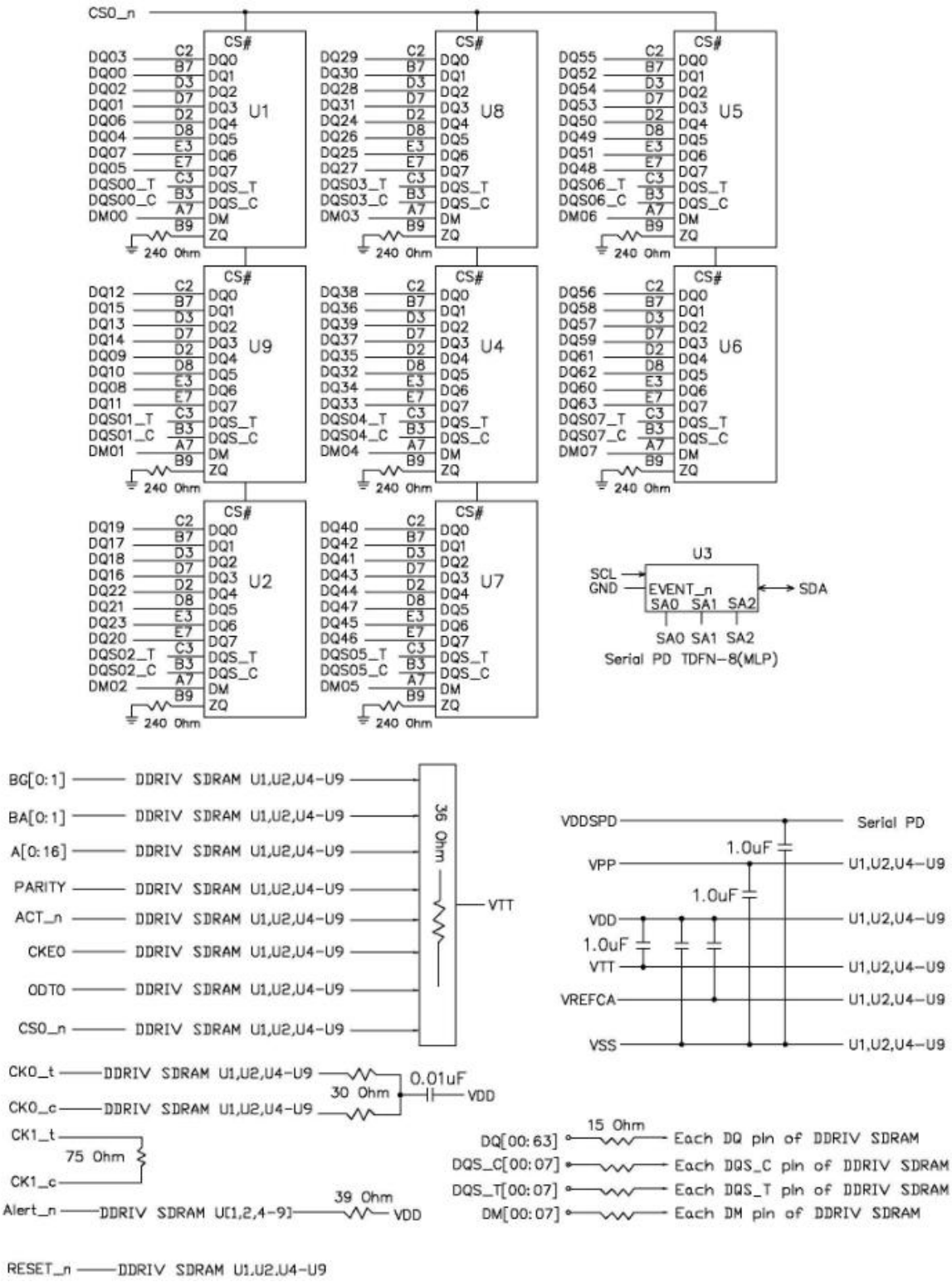
9. DQ Maps

Component-to-Module DQ Map

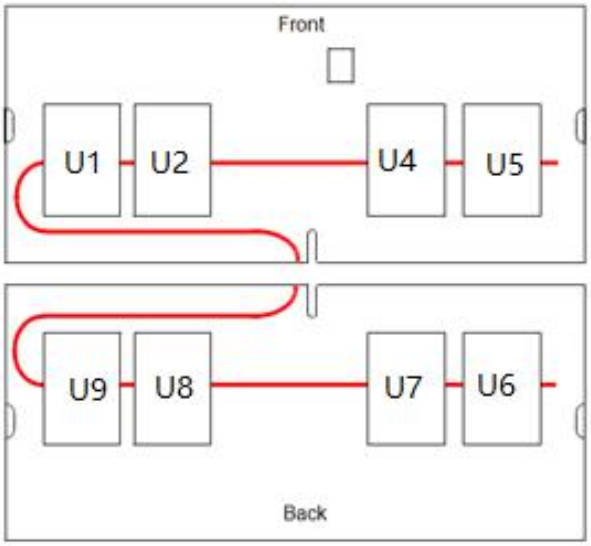
Component Reference Number	Module DQ	IC DQ	Module Pin Number	Component Reference Number	Module DQ	IC DQ	Module Pin Number
U1	0	1	8	U9	8	6	28
	1	3	7		9	4	29
	2	2	20		10	5	41
	3	0	21		11	7	42
	4	5	4		12	0	24
	5	7	3		13	2	25
	6	4	16		14	3	38
	7	6	17		15	1	37
U2	16	3	50	U8	24	4	70
	17	1	49		25	6	71
	18	2	62		26	5	83
	19	0	63		27	7	84
	20	7	46		28	2	66
	21	5	45		29	0	67
	22	4	58		30	1	79
	23	6	59		31	3	80
U4	32	5	174	U7	40	0	195
	33	7	173		41	2	194
	34	6	187		42	1	207
	35	4	186		43	3	208
	36	1	170		44	4	191
	37	3	169		45	6	190
	38	0	183		46	7	203
	39	2	182		47	5	204
U5	48	7	216	U6	56	0	237
	49	5	215		57	2	236
	50	4	228		58	1	249
	51	6	229		59	3	250
	52	1	211		60	6	232
	53	3	212		61	4	233
	54	2	224		62	5	245
	55	0	225		63	7	246

10. Functional Block Diagram

8GB Non ECC Module (Populated as 1 ranks of x8 DDR4 SDRAMS)

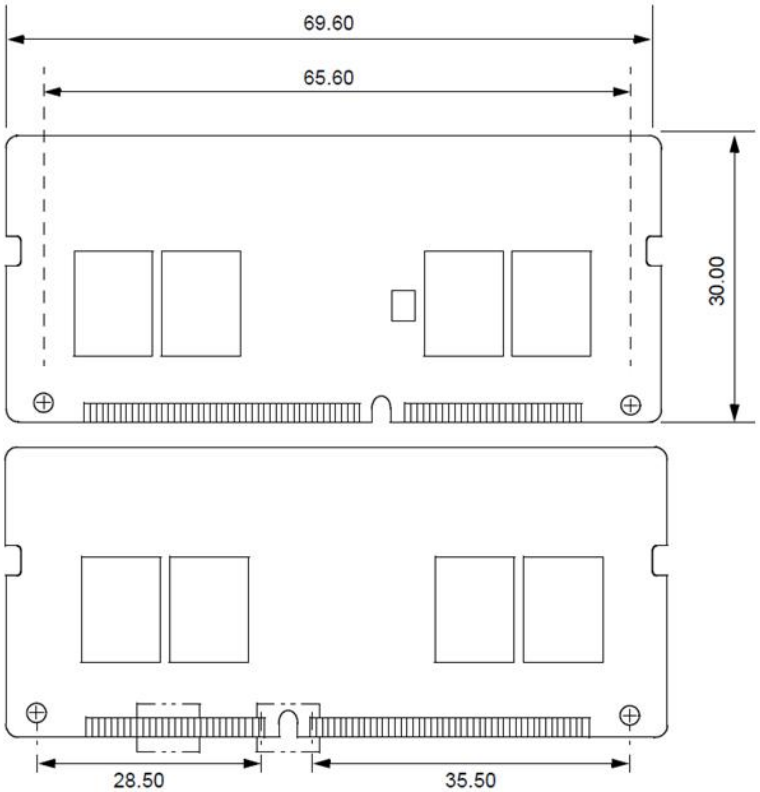


10. Functional Block Diagram



11. Module Dimensions

1Gig x8*8pcs Module (1 Rank) Physical dimensions:



Notes:

1. All dimensions are in millimeters.
2. The dimensional diagram is for reference only.
3. Tolerance on all dimensions ±0.15mm unless otherwise specified.

12. Revision History

Date	Revision	Description
Mar-2022	V1.0	Initial release